

REMARKS

Applicants request favorable reconsideration and allowance of the subject application in view of the preceding amendments and the following remarks.

To place the application in better form, Applicants submit herewith a substitute specification, which includes a new abstract. For the Examiner's convenience, also provided is a marked-up copy of the original specification showing the portions thereof which are being changed. The substitute specification includes the same changes as are indicated in the marked-up copy. Applicants' undersigned attorney has reviewed the substitute specification and submits that the substitute specification contains no new matter.

Claims 1-16 are presented for consideration. Claims 1, 4, 11, 12 and 15 are independent. Claims 1-11 have been amended to clarify features of the subject invention, while claims 12-16 have been added to recite additional features of the subject invention. Support for these changes and these claims can be found in the original application, as filed. Therefore, no new matter has been added.

Applicants note with appreciation that claims 1-10 have been allowed over the art of record. Applicants submit that the foregoing changes to claims 1-10 do not affect the allowability of these claims. Therefore, claims 1-10 should remain allowable. In addition these claims being allowable, Applicants submit that claims 11-16, as presented, patentably define features of the semiconductor device and the manufacturing method of the present invention. Applicants submit, therefore, that claims 11-16 also should be deemed allowable over the art of

record. Accordingly, Applicants request favorable reconsideration and withdrawal of the rejection set forth in the above-noted Office Action.

Claim 11 was rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,197,452 to Matumoto. Applicants submit that the cited art does not teach many features of the present invention, as previously recited in claim 11. Therefore, this rejection is respectfully traversed. Nevertheless, Applicants submit that claims 11-16, as presented, amplify the distinctions between the present invention and the cited art.

In one aspect of the present invention, independent claim 11 recites a semiconductor device having a plurality of wiring layers. The device includes a wiring, which is formed by a first wiring layer, formed by divisional exposure, a connecting position at the time of the divisional exposure formed in parallel with the wiring, which is formed by the first wiring layer, and a wiring, which is formed by a second wiring layer, having an area which intersects the connecting position.

In another aspect of the present invention, independent claim 12 recites a manufacturing method of manufacturing a semiconductor device having a plurality of wiring layers. The method includes steps of forming a wiring by a first wiring layer according to a divisional exposure, in which the wiring formed by the first wiring layer does not intersect a connecting position at the divisional exposure, and forming a wiring by a second wiring layer, in which at least a part of the wiring formed by the second wiring layer has an area intersecting the connecting position.

In still another aspect of the present invention, independent claim 15 recites a semiconductor device comprising wirings formed from a plurality of wiring layers including at least first and second wiring layers. The device includes a wiring, which is formed from the first wiring layer, formed according to a divisional exposure and not crossing over a connecting position at a divisional exposure, and at least a part of a wiring formed from the second wiring layer crossing over the connecting position.

Applicants submit that the cited art does not teach or suggest such features of the present invention, as recited in independent claims 11, 12 and 15.

The Matumoto patent relates to a light exposure pattern mask with dummy patterns, and a method of producing the mask. In that pattern, the light exposure pattern mask includes an integrated circuit wiring pattern consisting of a plurality of wiring pattern elements, and a dummy pattern consisting of a plurality of dummy pattern elements provided in the vicinity of ends of the wiring pattern elements. In more detail, in that patent, in order to prevent a tapering wiring end at an exposure position, and to prevent short-circuiting between wiring on a grid arranged at a predetermined interval, a dotted dummy pattern is formed separately from the wiring pattern.

Apparently, the Examiner takes the position that the grid 110 shown in that patent for explaining the dummy pattern formed on the grid arranged at a predetermined interval is another wiring layer from the wiring pattern 103. Applicants submit, however, that the dummy pattern and the wiring pattern 103 are merely shown schematically in order to explain the predetermined interval arrangement.

Specifically, Applicants submit that this arrangement is not a practical configuration of the arrangement of the wiring pattern.

Still further, apparently, the Examiner takes the position that the dot-shaped dummy pattern 101 is the connecting position at the divisional exposure. Applicants submit, however, that, in fact, the pattern element 101 is, as discussed above, the dot-shaped dummy pattern formed separately from the wiring pattern in order to prevent undesirable tapering of the wiring end at the exposure position and to prevent undesirable short-circuiting between the wiring. Applicants submit, therefore, that the pattern element 101 in the Matsumoto patent is quite different from the connecting position at the divisional exposure, in the manner of the present invention recited independent claim 11, for example. For these reasons, Applicants submit that the Matumoto patent does not teach or suggest salient features of Applicants' present invention, as recited in independent claim 11.

For reasons similar to those advanced above, Applicants further submit that the Matumoto patent does not teach or suggest salient features of Applicants' present invention, as recited in independent claims 12 and 15, including a wiring, which is formed from a first wiring layer, formed according to a divisional exposure, which does not interconnect a connecting position at the divisional exposure (independent claim 12), or does not cross over a connecting position at a divisional exposure (independent claim 15), or forming a wiring by a second layer, wherein at least a part of the wiring formed by the second wiring layer has an area intersecting the connecting position (independent claim 12), or at least a part of a wiring formed from a second wiring layer crossing over a connecting position (independent claim 15).

For the foregoing reasons, Applicant submits that the present invention, as recited in independent claims 11, 12 and 15, also is patentably defined over the cited art.

Dependent claims 13, 14 and 16 also should be deemed allowable, in their own right, for defining other patentable features of the present invention in addition to those recited in their respective independent claims. Further individual consideration of these dependent claims is requested.

Applicants further submit that the instant application is in condition for allowance. Favorable reconsideration, withdrawal of the rejection set forth in the above-noted Office Action and an early Notice of Allowance are requested.

Applicants' undersigned attorney may be reached in our Washington, D.C. office by telephone at (202) 530-1010. All correspondence should continue to be directed to our address given below.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Steven E. Warner", is written over a horizontal line.

Attorney for Applicants
Steven E. Warner
Registration No. 33,326

FITZPATRICK, CELLA, HARPER & SCINTO
30 Rockefeller Plaza
New York, New York 10112-3801
Facsimile: (212) 218-2200